This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A detector framing node receiving image data and communicating a portion of the image data to a host computer, comprising:

an image detection interface to receive image data in the form of at least one image frame having a predetermined sequence of event instructions constructed off-line~~size~~;

a control unit to select a predetermined portion of the image data received on execution of the predetermined sequence, for storage; and

a memory unit to store the predetermined portion in response to the selection by said control unit.

2. (Original) The detector framing node according to claim 1, wherein the rate of communication between said image detection interface and said memory unit is greater than or equal to the rate of reception of the image data by said image detection interface.

3. (Original) The detector framing node according to claim 1, wherein said control unit is programmable to receive the image data from a selected flat panel detector of a plurality of different flat panel detectors.

4. (Original) The detector framing node according to claim 3, wherein said control unit communicates the received image data to a host memory of the host computer independent of an operating system run by the host computer.

5. (Original) The detector framing node according to claim 4, wherein the host computer runs a non-real time operating system, and the detector framing node continues to receive and store the image data from the selected flat panel detector during a lapse in communication with the host memory.

6. (Original) The detector framing node according to claim 3, wherein the received image data is radioscopic image data and the selected flat panel detector includes an amorphous silicon photo-diode array outputting the radioscopic image data in response to detection of a radiographic image.

7. (Original) The detector framing node according to claim 1, wherein a plurality of image frames are received continuously by said image detection interface.

8. (Original) The detector framing node according to claim 7, wherein each image frame is at least a 1024 x 1024 array of 16 bit words of image data received at a rate of at least 30 frames/sec, or is at least a 2048 x 2048 array of 16 bit words of image data received at a rate of at least 7.5 frames/sec.

9. (Original) The detector framing node according to claim 1, further comprising:

a computer communication interface to communicate the image data stored in said memory unit to a host memory of the host computer,

wherein the image data is stored in the memory unit according to a first order and output to the host memory of the host computer according to a second order.

10. (Original) The detector framing node according to claim 9, wherein said detector framing node transfers the received data to the host memory as indicated by a list of physical addresses stored in registers in said detector framing node.

11. (Original) The detector framing node according to claim 1, wherein said image detection interface (376) receives the real time data at a rate of at least 60 Mbytes/sec.

12. (Original) The detector framing node according to claim 1, wherein the detector framing node is a PCI card and the host computer runs a non-real time operating system.

13. (Original) The detector framing node according to claim 1, wherein the detector framing node is a PCI card and the host computer runs a real time operating system.

14. (Original) The detector framing node according to claim 1, wherein the detector framing node is a PCI card and the host computer runs a task based operating system.

15. (Currently amended) An imaging system, comprising:

at least one host processor to execute operations with a host operating system;

a host memory to store image data;

a computer communication bus connecting said at least one host processor with said host memory;

an image detection interface to receive image data in the form of at least one image frame having a predetermined sequence of event instructions constructed off-line, from an image detection bus;

a detector memory unit to store the image data received by said image detection interface; and

a computer communication interface to communicate the stored image data from said detector memory unit to said host memory along said computer communication bus.

16. (Original) The system according to claim 15, further comprising:

a detector control unit to control communication of the image data between said image detection interface and said detector memory unit independently from the host operating system.

17. (Original) The system according to claim 16, wherein said detector control unit is programmable to receive the image data from a selected flat panel detector of a plurality of different flat panel detectors.

18. (Original) The system according to claim 17, wherein said detector control unit communicates the received image data to said host memory independent of the host operating system.

19. (Original) The system according to claim 15, wherein the image data is received by said image detection interface as an image frame, and the detector memory unit stores a predetermined portion of the image frame.

20. (Original) The system according to claim 19, wherein said detector memory unit only stores the predetermined portion from each image frame received by said image detection interface.

21. (Original) The system according to claim 15, wherein the rate of storage of the image data into said detector memory unit is greater than or equal to a rate of reception of the image data by said image detection interface.

22. (Original) The system according to claim 15, wherein the host operating system is a non-real time operating system, and said image detection interface continues to receive and store the image data from the image detection system during a lapse in communication with said host memory.

23. (Original) The system according to claim 15, wherein the image frames are received continuously by said image detection interface.

24. (Original) The system according to claim 15, wherein each image frame is at least a 1024 x 1024 array of 16 bit words of image data received at a rate of at least 30 frames/sec, or is at least a 2048 x 2048 array of 16 bit words of image data received at a rate of at least 7.5 frames/sec.

25. (Original) The system according to claim 15, wherein the image data is stored in said detector memory unit (380) according to a first order and output to said host memory according to a second order.

26. (Original) The system according to claim 15, wherein said computer communication interface transfers the image data to said host memory as indicated by a list of physical addresses stored in a plurality of registers.

27. (Original) The system according to claim 15, wherein said image detection interface receives the image data at a rate of at least 60 Mbytes/sec.

28. (Original) The system according to claim 15, wherein said image detection interface, said detector memory unit, and said computer communication interface are disposed on a PCI card and the host operating system is a non-real time operating system.

29. (Original) The system according to claim 15, wherein said image detection interface, said detector memory unit, and said computer communication interface are disposed on a PCI card and the host operating system is a real time operating system.

30. (Original) The system according to claim 15, wherein said image detection interface, said detector memory unit, and said computer communication interface are disposed on a PCI card and the host operating system is a task based operating system.

31. (Original) The system according to claim 15, wherein the received image data is radioscopic image data and the image detection bus receives the image data from a flat panel detector.

32. (Original) The system according to claim 31, wherein the flat panel detector is selected from a plurality of flat panel detectors having different image data output format.

33. (Original) The system according to claim 15, wherein the image data is radioscopic image data (316) received by said image detection interface at a rate of at least 1 Gbit/sec.

34. (Currently amended) An imaging system, comprising:

a host computer comprising at least one host processor to and a host memory connected to the at least one host processor with a computer communication bus; and

a card connected to the computer communication bus to receive image data <u>in the form of at least one image frame having a predetermined sequence of event instructions constructed off-line,</u> from an image detection bus from an image detection bus at a first clock frequency and to communicate the received image data to the host memory through the computer communication bus at a second clock frequency different than the first clock frequency.

35. (Original) The system according to claim 34, wherein said card selectably receives at least a 1024 x 1024 array of 16 bit words of image data at a rate of at least 30 frames/sec or at least a 2048 x 2048 array of 16 bit words of image data at a rate of at least 7.5 frames/sec.

36. (Original) The system according to claim 34, wherein the image detection bus receives the image data at a rate of at least 60 Mbytes/sec.

37. (Original) The system according to claim 34, wherein said card communicates the image data to the host memory along the computer communication bus at a data rate of at least 33 MHz.

38. (Original) The system according to claim 37, wherein the computer communication bus is a PCI bus.

39. (Currently amended) A detector framing node to receive image data in the form of at least one image frame having a predetermined sequence of event instructions constructed off-line, forming an image of predetermined size and to communicate the received image data with a host computer having at least one host processor and a host memory, comprising:

an image detection interface to receive the image data;

a plurality of frame buffer memory units, each having a corresponding predetermined data storage capacity; and

a control unit to select a predetermined portion of the image for storage into a selected frame buffer memory unit of said plurality of frame buffer memory units.

40. (Original) The detector framing node according to claim 39, wherein said control unit is programmable to receive the image data from a selected flat panel detector of a plurality of different flat panel detectors (116), wherein each of the different flat panel detector outputs a corresponding differently sized image.

41. (Original) The detector framing node according to claim 39, wherein said control unit communicates the received image data to the host memory of the host computer independent of a host operating system.

42. (Original) The detector framing node according to claim 39, wherein the rate of storage of the image data (316) into said plurality of frame buffer memory units is a rate greater than or equal to a rate of reception of the image data by said image detection interface.

43. (Original) The detector framing node according to claim 39, wherein each image frame is at least a 1024 x 1024 array of 16 bit words of image data received at a rate of at least 30 frames/sec.

44. (Original) The detector framing node according to claim 39, wherein the image data is stored in said detector memory unit according to a first order and output to said host memory according to a second order.

45. (Original) The detector framing node according to claim 39, wherein the image detection bus receives the image data at a rate of at least 60 Mbytes/sec.

46. (Original) The detector framing node according to claim 39, wherein said card communicates the image data to the host memory along the computer communication bus at a data rate of at least 33 MHz.

47. (Original) The detector framing node according to claim 39, wherein the portion of the image selected by said control unit is less than or equal to the predetermined storage capacity of each of the plurality of frame buffer memory units.